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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/825,941	04/05/2001	Masahiko Honda	0050-0093	3805

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EXAMINER	
SHAH, CHIRAG G	

ART UNIT	PAPER NUMBER
2664	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/825,941	HONDA, MASAHIKO	
	Examiner	Art Unit	
	Chirag G. Shah	2664	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 15-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 15-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's argument with respect to the double patenting rejection in view of Matsumura is withdrawn.

2. Applicant's arguments with respect to claims 1-9 and 15-18 have been considered but are moot in view of the new ground(s) of rejection.

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-9 rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura et al (U.S. Patent No. 6,269,077), hereinafter, Matsumura in view of Yamada et al. (U.S. Patent No. 6,400,718), hereinafter Yamada.

Regarding claim 1, Matsumura discloses a redundant system having two switch routes [see claim 2, lines 1-3, U.S. Patent No. 6269077], comprising:

N, with N greater than or equal to one, input selectors [N=1 input selector, see claim 2, lines 4 and fig. 1], each for receiving an input line and for connecting the received input line to one of two switch routes [see fig. 1, where when N=1, the input selectors receive input signal and the N input selector selects the system currently being operated];

a switch section (temporary cell storage unit 20, see fig. 1) of two switch routes (active system and standby system routes, see fig. 1), each of the switch sections having N input portions and N output ports (see fig. 1), and N buffers (see fig. 2) [a temporary cell storage unit is in each active and stand-by system that includes N buffers, see claim 2, lines 8-11 and see fig. 1 and 2] that each further include,

M, with M greater than or equal to two, priority queues for storing packets having different priorities [see claim 2, lines 8-15 and fig. 2 and-3 for temporary cell storage units for receiving and storing delay priority in temporary storage units received from an input selector classified with a delay priority. Note there are 2 or more priority queues in fig. 3];

an output selector [claim 2, lines 6-7] for selecting one of the M priority queues from one of the N buffers of one of the two switch sections [see combination of fig. 2 and fig. 3, where the output selector may select the one of the M highest delay priority classes from one of the N buffers of one of the two switches];

a controller configured to receive status signals from both of the switch sections that include information relating to a packet storing status of the M priority queues and, based on the status signals, control the output selector to select the one of the M priority queues [see claims 2, lines 12-20 and 6-7 and col. 5, lines 35-46, and figs. 1 and 2, a one of two control means having status signals for instructing one of temporary cell storage units having the highest delay priority to read out the cell and for outputting the read out cell from one of temporary cell storage to the output selector and means for arbitrating cell reading from which temporary cell storage unit is to be performed depending on the cell storage condition].

Matsumura discloses in fig. 1 of two different control means with respect to the active and standby receiving status messages. *Matsumura fails to explicitly disclose of a single controller configured to receive status signals from both of the switch sections to include information relating to a packet storing status and additionally the controller generates the system switching signal, which is used by the input selector for connecting the input line to one of the two switch routes.*

Yamada teaches of hit-less switching between an active system and a standby system. Yamada figs. 1 and 5 and col. 6, lines 53 to col. 7, lines 33 of a single controller 12 capable of receiving queue buffer vacancy and fill-level. The controller 12 is also capable of setting up an

in-switching condition. Furthermore, as disclosed in col. 5, lines 55-65, the single controller 12 is operational for both active and standby system and is further executes switching control by interchanging signal with the control circuit of the selector, thus clearly suggesting that the interchanging signal is used by the input selector for connecting the input line to one of the two switch routes. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Matsumura to include the features of a signal controller that generates the system switching signal to be used to connect input line to one of two switch routes as taught by Yamada. One is motivated as such in order to execute accurate available bit rate control despite hit-less switching, assuring an achievement to meet various traffic control demands.

Regarding claim 5, Matsumura discloses in fig. 1 of a packet switching system having two switch routes, comprising:

N, with N greater than or equal to one, input selectors [for N=1, Input selector 10, see fig. 1], each of which selects a one of two switch routes to connect N lines to the selected one based on incoming signal [the input selector selects the active system based on the incoming cell flow signal, see fig. 1 and col. 4, lines 40-50];

A switch section [active and stand-by systems, see fig. 1], one provided for each of the two switch routes, each of the switch sections having N input ports and N output ports and comprising N buffers [each system includes input port and output port and temporary cell storage (buffer) unit, see fig. 1], each of the N buffers further including

a high-priority queue for storing input packets having a high priority [each temporary storage unit includes Delay priority m queue, where m>n see fig. 2; the high priority queue receives data from input selector 10, see fig. 1]; and

a low-priority queue for storing input packets having a low priority [each temporary storage unit includes Delay priority N queue, where m>n see fig. 2; the low priority queue receives data from input selector 10, see fig. 1];

a high-priority output selector coupled to the high-priority queues in each of the switch sections [Delay Priority Selector 40 and 50 coupled to delay priority queue m, see fig. 2];

a low-priority output selector coupled to the low-priority queues in each of the switch sections [Delay Priority Selector 40 and 50 coupled to delay priority queue n, see fig. 2];

a high priority output queue for storing an output of the high-priority output selector [output selector for delivery of cells by selecting one high-priority queues of a system; output selector inherently includes a queues for storing the selected units, see fig. 1 and col. 5, lines 46-66];

a low-priority output queue for storing an output of the low-priority output selector [output selector for delivery of cells by selecting one low-priority queues of a system; output selector inherently includes a queues for storing the selected units, see fig. 1 and col. 5, lines 46-66]; and

a controller configured to receive status signals from both of the switch sections that include information relating to a storage status of the high-priority queues and the low-priority queues, the controller controlling the high-priority output selectors and the low-priority output selectors [see claims 2, lines 12-20 and 6-7 and col. 5, lines 26-46, 57-67, and figs. 1 and 2, a one

of two control means having status signals for instructing one of temporary cell storage units having the highest delay priority to read out the cell and for outputting the read out cell from one of temporary cell storage to the output selector and means for arbitrating cell reading from which temporary cell storage unit is to be performed depending on the cell storage condition].

Matsumura discloses in fig. 1 of two different control means with respect to the active and standby receiving status messages. *Matsumura fails to explicitly disclose of a single controller configured to receive status signals from both of the switch sections to include information relating to a packet storing status and additionally the controller generates the system switching signal, which is used by the input selector for connecting the input line to one of the two switch routes.*

Yamada teaches of hit-less switching between an active system and a standby system. Yamada figs. 1 and 5 and col. 6, lines 53 to col. 7, lines 33 of a single controller 12 capable of receiving queue buffer vacancy and fill-level. The controller 12 is also capable of setting up an in-switching condition. Furthermore, as disclosed in col. 5, lines 55-65, the single controller 12 is operational for both active and standby system and is further executes switching control by interchanging signal with the control circuit of the selector, thus clearly suggesting that the interchanging signal is used by the input selector for connecting the input line to one of the two switch routes. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Matsumura to include the features of a signal controller that generates the system switching signal to be used to connect input line to one of two switch routes as taught by Yamada. One is motivated as such in order to execute accurate

available bit rate control despite hit-less switching, assuring an achievement to meet various traffic control demands.

Regarding claim 2, wherein when the one of the two switch routes is switched to an other switch route [system switching control means comprises a system-switching control units as disclosed in col. 2, lines 32-65], the controller monitors a packet storing status of each of the high-priority and low-priority queues [system-switching control unit 21 or 31, in each system mutually communicates with each other and manages a temporary cell storage nit, in which cells to be read out are stored in accordance with the delay priority group as disclosed in figure 1 and abstract] and, when one of the high-priority queues corresponding to respective ones of the two switch sections becomes empty, then the controller instructs the high-priority output selector to select the other of the two high-priority queues to store an output of the selected one of two M priority queues (the high-priority output queue) in a one of two switch sections into the high-priority output queue [as disclosed in column 2, lines 18-48, column 4, lines 57-59, column 5, lines 35-46, control means for arbitrating cell reading form which temporary cell storage unit is to be performed depending on cell storage condition] as claims.

Regarding claim 3, Matsumura discloses that the switch section further comprises a readout controller [read control unit 204 in figure 3] controlling a packet reading sequence of the high-priority and low-priority queues for each of the N buffers such that priority in packet reading is given to the high-priority queue [as disclosed in figure 1, 3 and in column 5, lines 4-16, the system-switching control unit 21 instructs to the temporary cell storage unit 20 to read

out cells in the order of higher delay priority. Thus cells are read out successively in he order of their delay priorities] as claims.

Regarding claim 4, Matsumura discloses wherein the controller instructs the output selector to sequentially select the M priorities in descending order of priority [as disclosed in column 5, lines 4-16, 35-52 that the system-switching control instructs the output selector to read out cells from the temporary cell storage unit in the order of higher delay priority] as claim.

Regarding claim 6, wherein when a one of the two switch routes is switched to an other switch route by the system switching signal [system switching control means comprises a system-switching control units as disclosed in col. 2, lines 32-65], the controller monitors a packet storing status of each of the high-priority and low-priority queues [system-switching control unit 21 or 31, in each system mutually communicates with each other and manages a temporary cell storage nit, in which cells to be read out are stored in accordance with the delay priority group as disclosed in figure 1 and abstract] and, if one of the high-priority queues corresponding to respective ones of the two switch sections becomes empty, then the controller instructs the high-priority output selector to select an other of the two high-priority queues to store an output of the selected one of two M priority queues (the high-priority output queue) in a one of two switch sections into the high-priority output queue [as disclosed in column 2, lines 18-48, column 4, lines 57-59, column 5, lines 35-46, control means for arbitrating cell reading form which temporary cell storage unit is to be performed depending on cell storage condition] as claims.

Regarding claim 7, Matsumura discloses that the switch section further comprises a readout controller [read control unit 204 in figure 3] controlling a packet reading sequence of the high-priority and low-priority queues for each of the N buffers such that priority in data unit reading is given to the high-priority queue [as disclosed in figure 1, 3 and in column 5, lines 4-16, the system-switching control unit 21 instructs to the temporary cell storage unit 20 to read out cells in the order of higher delay priority. Thus cells are read out successively in he order of their delay priorities] as claims.

Regarding claim 8, Matsumura discloses wherein the readout controller starts reading out low-priority data units stored in the low-priority queue after all high-priority data units stored in the high priority queue have been completely read out [as disclosed in column 5, lines 4-16 and in column 6, lines 57-64, once all cells in the same priority group (high priority) have been read out, then cells in the next priority order group are to be read out] as claim.

Regarding claim 9, Matsumura discloses wherein the readout controller controls a packet reading sequence of the high-priority and low-priority queues for each of the N buffers such that m high-priority data units are read out from the higher-priority queue and n low-priority packets are read out from the low-priority queue, wherein m is set to be greater than n [see, column 5, liens 4-16, fig. 2 and claim 2].

6. Claims 15-18 rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (U.S. Patent No. 6,400,718), hereinafter Yamada in view of Matsumura et al (U.S. Patent No. 6,269,077), hereinafter, Matsumura.

Regarding claim 15, Yamada discloses in figure 1 of a switching system comprising:

a plurality of input selector switches [input ports 24, 26, 28, 30, 32, 34 see fig. 1] each configured to be connected to an input line [input cell gate 36, fig. 1], and each receiving a system switching signal [see col. 5, lines 55-64, the controller 12 sends an "active" command or a "standby" command];

a first switch section and a second switch section connected to the plurality of input selector switches [see fig. 1], one of the first switch section or the second switch section receiving packets from the plurality of input selector switches in response to the system switching signal indicating that either the first switch section or the second switch section is active [see fig. 1 and col. 5, lines 55-64], the first and second switch sections each including a buffer corresponding to each of the input selector switches [see fig. 5 and col. 6, lines 53 to col. 7, lines 33],;

a plurality of output selectors [output port, see fig. 1] each connected to one of the buffers from the first and second switch sections [see col. 6, lines 33-65 and fig 1]; and

a controller (controller 12, fig. 1 and 5) configured to generate the system switching signal and to receive status signals from the first switch section and the second switch section that include information relating to a state of the first switch section and the second switch

section and being used by the controller to control the plurality of output selectors [see col. 6, lines 53 to col. 7, lines 33].

Yamada fails to explicitly disclose each of the buffers further including a plurality of priority queues for storing different priority packets from corresponding ones of the input selector switches.

Matsumura teaches a system switching over apparatus for duplicated ATM switch, which enables keeping the delay quality of each cell unchanged without any cell loss, are realized. Matsumura discloses in claim 2, lines 8-15 and fig. 2 and 3 for temporary cell storage units (buffer) for receiving and storing delay priority in temporary storage units received from an input selector classified with a delay priority. Note there are 2 or more priority queues in fig. 3. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to modify the teachings of Yamada to include the buffer including priority queues for storing different priority packets from corresponding ones of the input selector switches as taught by Matsumura. One is motivated as such in order to provide quality of service for higher delay priority cells over lower delay priority cells.

Regarding claim 16, Yamada fails to explicitly disclose wherein the plurality of output selectors are controlled to receive packets from one of the priority queues corresponding to the buffer to which an output selector is connected. Matsumura discloses in the combination of figures 2 and 3 that output selectors are controlled to receive packets from delay priority m or delay priority n from the buffer to which an output selector is connected with. Therefore, it would have been obvious to one of ordinary skills in the art at the time of the invention to

modify the teachings of Yamada to include the buffer including priority queues for storing different priority packets from corresponding ones of the input selector switches as taught by Matsumura. One is motivated as such in order to provide quality of service for higher delay priority cells over lower delay priority cells

Regarding claim 17, Yamada discloses based on fig. 1 wherein the input selector switches [24, 26, 28, 30, 32, 34, see fig. 1] are each connected to an input line via an input processor [cell gate processor circuitry 36] as claim.

Regarding claim 18, Yamada illustrates in fig. 1 wherein a number of the output selectors [48-56 input port, see fig. 1] is equal to a number of the input selector switches [36-46 input ports, see fig. 1] as claim.

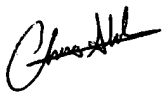
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G. Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 571-272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cgs
February 19, 2006



Chirag Shah
Patent Examiner